

**VIRTUAL EVENT**

**EMC Compo 2021**  
October 26-29, Bruges, Belgium  
now **March 9-11, 2022**



## SCHEDULE AT A GLANCE

<b>Wednesday, 9<sup>th</sup> March 2022</b>	
CET 9h 30 – 10h 45	<b><u>Opening session &amp; Welcome remarks</u></b> Prof. dr. ir. Davy Pissoort <i>General chair, EMC Compo 2021</i> <b><u>Plenary session</u></b> “ <b>To shield or to absorb?</b> ” Prof. dr. ir. Frank Leferink <i>Chair EMC, University of Twente</i>
11h 15 – 12h 30	<b><u>Discussion Forum</u></b> “ <b>Roadmap on EMC at IC Level</b> ” Dr. Frederic Lafon, <i>Valeo</i> Prof. Dr. Mohamed Ramdani, <i>ESEO</i>
13h 30 – 14h 50	<b><u>Technical session</u></b> Design Techniques -1
15h 00 – 16h 00	<b><u>Technical session</u></b> IC Emissions - 1
16h 30 – 18h 00	<b>Exhibitors Presentation</b>
<b>Thursday, 10<sup>th</sup> March 2022</b>	
9h 30 – 10h 45	<b><u>Plenary session</u></b> Dr. Bart Boesman, <i>Melexis</i>
11h 15 – 12h 15	<b><u>Technical session</u></b> IC Emissions - 2
13h 30 – 14h 50	<b><u>Technical session</u></b> Design techniques - 2
15h 20 – 16h 40	<b><u>Technical session</u></b> IC Immunity - 1
16h 40 – 17h 30	<b><u>Special session</u></b> Discussion Forum
<b>Friday, 11<sup>th</sup> March 2022</b>	
9h 30 – 10h 30	<b><u>Technical session</u></b> IC Immunity - 2
10h 40 – 12h 00	<b><u>Technical session</u></b> PETER Project
13h 00 – 14h 40	<b><u>Technical session</u></b> New Design Methodologies
15h 00 – 16h 00	<b><u>Tutorial Session</u></b> “ <b>Board-Level-Shielding (BLS)</b> ” Prof. Dr. Andy Marvin, <i>University of York</i>
16h 00 – 16h 15	<b><u>Closing ceremony</u></b> Prof. dr. ir. Davy Pissoort, <i>KU Leuven</i>

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## WELCOME ADDRESS

**Chair: Prof. dr.ir. Davy Pissoort, *KU Leuven, Belgium***  
**Prof. Etienne Sicard, *INSA Toulouse***

### Dear participant of EMC COMPO 2021

A virtual welcome to our Medieval city of Bruges.

When the decision was taken to postpone EMC Compo from autumn 2021 to the springtime of 2022, we all hoped that this would be a “normal” physical symposium, with all typical actions related to this. We not only think about the live presentations of the papers and the following live discussions, but also about the informal contacts between participants, during the coffee breaks, or at evening during the social events, or even during some spare time during which we would be enjoying a good glass of the local beer “Brugse Zot”...

Nevertheless, a very warm welcome to all of you, spread over the whole world. We are bringing the symposium to you in a virtual format. And we are sure that the program contains many high level contributions. There are the two plenary sessions “To shield or to absorb” by Prof. F. Leferink and “ICs for the future” by Dr. B. Boesman. There are also the two keynote contributions “Roadmap on EMC at IC level” by Dr. Lafon and Prof. Ramdani, and “Board Level Shielding” by Prof. A. Marvin. But the most important part of the symposium are all papers presented in the different sessions, and where researchers are sharing their latest results within this community.

A special attention is also drawn to the discussion forum on Thursday in the afternoon, and the session on Wednesday afternoon, where the exhibitors will present the newest high technological measuring and test equipment.

We thank the local organizing committee, who did all the administration and organization in first delaying and then transforming this symposium from physical into a virtual one, the program committee, all members of the review board and all exhibitors who supported this symposium.

We hope that you enjoy this symposium, and besides all technological and research topics of this symposium, perhaps you will find some time to visit our historical medieval town at [Virtual Brugge, the official Poppr 360 virtual tour of Bruges \(virtualbruges.com\)](#)



Prof. Davy Pissoort  
(Chair of EMC COMPO 2021)



Prof. em. Johan Catrysse  
(Vice-chair of EMC COMPO 2021)

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**9<sup>th</sup> March 2022 9h30 - PLENARY SESSION**

**“ To shield or to absorb? ”**

**Prof. ir. dr. Frank Leferink, *Chair EMC - University of Twente  
Ambassador’s Chair, KU Leuven Bruges and Kulak campus***

**Chair: Prof. dr.ir. Davy Pissoot, *KU Leuven, Belgium***

**Prof. em. dr. Johan Catrysse, *KU Leuven, Belgium***



IEEE Fellow Prof.dr.ir. Frank Leferink has been with **THALES** in the Netherlands since 1984, where he is responsible for the EMC activities for the development of new radar systems and naval platforms. He is also manager of the Network of Excellence for EMC of the THALES group. THALES is sponsoring his part-time, full-research, professor position at the **University of Twente**, where Frank is holding the Chair for EMC. Twenty-two PhD researchers, two assistant-professors and several master students are currently active in the EMC group. Frank is member of the Board of Directors of the IEEE EMC Society and associate editor of the IEEE Transactions on EMC and the new IEEE Letters on EMC Practice and Applications. He also holds the **Ambassador’s Chair at KU Leuven Bruges and Kulak campus**.

**Abstract:**

Modern equipment is nearly always shielded and is using higher frequencies, thus smaller wavelengths. If the wavelength becomes smaller than the dimensions of a shielded enclosure, the fields will resonate which creates large amplitude variation inside the shielded enclosures, resulting in a drastic decrease of the shielded effectiveness. Any practical shielded enclosure needs a door, or a hatch, or a cap which is connected via screws, rivets, gaskets etc. The distance between any electrically connection shall be small that 1/100 of a wavelength, resulting in extremely short distances between screws, or very high requirements for gasket and compression. If we can decrease the field intensity inside the shielded enclosure, we can relax the strict requirements about those 1/100th short distances. Or even simple, we do not need a shielded enclosure anymore, but we need absorbers. Several examples of absorption compared to shielding will be shown. When to absorb and delete the shield: that’s the question...

**9<sup>th</sup> March 2022 11h15 - DISCUSSION FORUM**

**“Roadmap on EMC at IC level”**

**Dr. Frederic Lafon, *Valeo, France***

**Chair : Dr. ing. Tim Claeys, *KU Leuven, Belgium***

**Dr. Mohammed Ramdani, *ESEO, France***

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## 9<sup>th</sup> March 2022 TECHNICAL SESSION : DESIGN TECHNIQUES 1

Chair : **Prof. em. dr. Johan Catrysse, KU Leuven, Belgium**

**Dr. Bernd Deutschmann, TU Graz, Austria**

**13h30**

### **Characterization of the Shielding Effectiveness of Board-Level Shields using a Dedicated Stripline Test Method up to 44GHz**

Pavithrkrishnan Radhakrishnan, Tim Claeys, Johan Catrysse, Davy Pissoort

*KU Leuven, Belgium*

**Abstract:**

This paper reports on the characterization of the Shielding Effectiveness (SE) of Board Level Shielding (BLS) components up to 44 GHz, using a dedicated stripline measuring setup. The setup is based on a similar measuring method for the characterization of shielding gaskets, as described in SAE ARP 6248. In this paper, the SE of both BLS components and the mounting technique on a Printed circuit board (PCB) can be characterized using this stripline setup. The measurements show the effect on the SE values due to the fact that the ground (GND) layer is embedded in a multilayer PCB, forming a slit between this GND layer and the BLS component. Techniques, based on a waveguide beyond cut-off (WGBC) by an appropriate use of multiple vias, are evaluated using this dedicated stripline setup.

**13h50**

### **Influence of Layout Parasitics on EMI Improved Folded Cascode Amplifier Input Stages using Compensation methods**

Dominik Zupan, Nikolaus Czepl, Bernd Deutschmann

*Graz University of Technology, Austria*

**Abstract:**

In this work we examine the electromagnetic interference (EMI) behaviour of EMI improved integrated folded cascode amplifier input stages. In that regard we compare three EMI improved differential input pair structures. These structures use the concept of compensation to decrease EMI susceptibility. We put special focus on the differences in the behaviour of the structures at the design stage and the layout stage. Therefore, we consider layout-specific parasitics, that may affect circuit performance. The performance parameters include EMI induced offset voltage, electromagnetic interference rejection ratio (EMIRR), layout considerations, differential and common mode gain, gainbandwidth product (GBWP), stability, power consumption, area requirement (estimation vs. implementation).

**14h10**

### **Resonance Property of a Novel Vertical Substrate Integrated Waveguide**

Yu-Ru Feng, Xing-Chang Wei, Qi-Han Xiao, Shen-Quan Liu, Cong-De Luo, Zhi-Ying Zhang

*Zhejiang University, China*

**Abstract:**

Millimeter-wave communication plays a more and more important role in electronic industry. The request for transmission structure is more complex and diversified accordingly. A novel vertical substrate integrated waveguide structure (VSIW) based on multi layers printed circuit board (PCB) is analyzed in this paper. It is composed of substrate, vias and multi copper layers with etched rectangular holes. When top and bottom layers' etched holes shift along the short side of the holes, in the frequency band of 75 GHz to 90 GHz, the cavity resonance mode maybe excited. This will greatly degenerate the propagation of the signal. It is proved that this resonance phenomenon is due to that the propagation TE<sub>10</sub> mode converts to the cavity resonant TM<sub>110</sub> mode. Furthermore, an empirical formula for predicting the TM<sub>110</sub> mode resonance frequency using the curve fitting method is proposed. It can fast predict the resonance frequency without time-consuming simulation. The accuracy of the predicted formula is verified by several six-layer VSIW simulation examples.



**14h30**

### **Electromagnetic Impact of Interconnect Resistance on STDP Characteristics in Neuromorphic Crossbar Array**

Tuomin Tao<sup>1</sup>, Hanzhi Ma<sup>1</sup>, Quankun Chen<sup>1</sup>, Shurn Tan<sup>1</sup>, En-Xiao Liu<sup>2</sup>, Er-Ping Li<sup>1</sup>

<sup>1</sup>Zhejiang University, China, People's Republic of ; <sup>2</sup>A\*STAR, Singapore

**Abstract:**

This paper presents an unsupervised-learning spiking neural network model based on spike-timing-dependent plasticity (STDP), which is then mapped into a neuromorphic crossbar array. Furthermore, the electromagnetic impact of the interconnect resistance on the STDP performance in the crossbar array is analyzed.

## **9<sup>th</sup> March 2022 TECHNICAL SESSION : IC Emission 1**

**Chair : Dr. ing. Tim Claeys, KU Leuven, Belgium**

**Mr. Renaud Gillon, ON Semiconductor**

**15h00**

### **Reduction of the Electromagnetic Emission from ICs using Soft Flexible Ferrite Sheets**

Bernd Deutschmann<sup>1</sup>, Junaid Shakeel Khan<sup>1</sup>, Gunter Winkler<sup>1</sup>, Jorge Victoria<sup>2</sup>

<sup>1</sup>Graz University of Technology, Austria; <sup>2</sup>Würth Elektronik eiSos GmbH & Co.KG, Germany

**Abstract:**

Soft ferrite sheets are widely used to reduce e.g. unwanted electromagnetic emissions from electronic systems. Based on standardized measurement procedures, the attenuation properties of different materials and thicknesses of such ferrite sheets can be investigated over a wide frequency range. The results of the measurements can be used to find the right ferrite plates for targeted reduction of electromagnetic interferences. In this paper, we characterize different ferrite sheets by measuring the coupling between two antennas according to a standardized measurement procedure as defined in IEC 62333. Furthermore, these ferrite sheets are applied to the surface of an IC package and various IC-level measurements are used to demonstrate the real electromagnetic emission reduction that can be achieved with these ferrite plates. Thereby reduction of the near E- and H-field are measured with near-field probes. Additionally, the reduction of the emissions obtained with the TEM-cell and the IC stripline method are considered. Finally, we will also discuss the influence of ferrite sheets on the conducted emission of an IC.

**15h20**

### **Measurements of Electromagnetic Emission inside Industrial Unmanned Aerial Vehicles**

Koh Watanabe<sup>1</sup>, Mai Aoi<sup>2</sup>, Misaki Komastu<sup>2</sup>, Satoshi Tanaka<sup>1</sup>, Makoto Nagata<sup>1</sup>

<sup>1</sup>Graduate School of Science, Technology, and Innovation, Kobe University, Japan ; <sup>2</sup>Graduate School of System Informatics, Kobe University, Japan

**Abstract:**

Unmanned aerial vehicles (UAVs) have been spread into various markets, such as logistics. The UAVs are requested to be safely flying above densely populated areas. Electromagnetic interference (EMI) problems can become prominent within their compact chassis where multiple electronic modules are densely packed. This paper presents the EMI evaluation between IC chips and wireless communications inside an industrial UAV. Also the two main sources of electromagnetic (EM) waves, power modules and control modules, are explored in respective dominant frequency ranges with near-field EM measurements up to 5 GHz. The influence on cellular communication performance was evaluated with a wireless communication system level simulator, predicting the degradation by 9 dB in the minimum receiver sensitivity of long-term evolution (LTE) communication system even if a receiver module is mounted at 200 mm distance in the chassis.



**15h40**

**Effects of SiC MOSFET Terminal Capacitances Evolution after Short-Circuit Aging tests on Conducted EMI in a Boost Converter**

Chawki Douzi<sup>1</sup>, Moncef Kadi<sup>1</sup>, Jaleddine Ben Hadj Slama<sup>2</sup>

<sup>1</sup>ESIGELEC, France ; <sup>2</sup>ENISO, Tunisie

**Abstract:**

Firstly, this paper presents the effect of short-circuit aging test on the electrical characteristics of Silicon Carbide (SiC) MOSFET. Experimental test is detailed and the evolution of parasitic input, output, reverse transfer capacitances ( $C_{iss}$ ,  $C_{oss}$  and  $C_{rss}$ ) is presented. Moreover, three capacitances between terminals, drain-source, gate-source and gate-drain capacitances ( $C_{ds}$ ,  $C_{gs}$  and  $C_{gd}$ ) are evaluated before and after repetitive short-circuit aging test. Secondly, in order to verify if the variation of these capacitances after aging can influence the Electromagnetic Interferences (EMI), we present a comparison of the EMI generated by a DC-DC boost converter before and after repetitive short-circuit aging test. Therefore, this work presents an experimental study of the short-circuit aging effect on the C-V characterization of SiC MOSFET to evaluate its electromagnetic behavior after degradation.

**9<sup>th</sup> March 2022 16h30 EXHIBITORS PRESENTATION**  
**Chair: Prof. dr.ir. Davy Pissort, KU Leuven, Belgium**  
**Dr. Anne Roc'h, TU Eindhoven, Netherlands**

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**10<sup>th</sup> March 2022 9h30 - PLENARY SESSION**

**“ A global IC development oriented approach towards Electromagnetic Compatibility : from concept design to final product release”**

**Dr. Bart Boesman, Melexis, Belgium**

**Chair: Prof. dr.ir. Davy Pissoot, KU Leuven, Belgium**



Bart Boesman was born in 1986. He received the M.S. degree in electrical engineering from the University College Katholieke Hogeschool Sint-Lieven, Ghent, Belgium, in 2009. In 2016, he received the Ph.D. degree in electrical engineering, at KU Leuven, Leuven, Belgium, where his focus was on computational electromagnetics and simulation tools for efficient system-level EMC analysis. In 2017, he joined Melexis Technologies NV, Tessenderlo, Belgium, where he is currently a Senior EMC System engineer. In his role he is supporting and steering the EMC modelling and simulation strategy for automotive ICs, and acting as an expert toward the design, application and compliance teams in order to continuously improve the EMC behavior of automotive ICs. He is also active as a member of the International Electrotechnical Commission Subcommittee 47A (IEC SC47A), participating to developments in IC-level EMC measurement methods and IC-level behavioral modelling approaches.

**Abstract:**

Any product which is placed onto the market, should not cause electromagnetic interface to surrounding receivers, but should also keep its own functionality under the presence of a possible disturbance source. When applied to automotive semiconductor products, this very vague but necessary requirement needs refinement into a set of low-level requirements which can easily be validated during the product's life cycle, from concept design to product release.

At the concept design stage, these requirements will define restrictions on e.g. technology, floorplan, and package design. At this stage, EMC design and system expertise play a crucial role, supported by a well-defined simulation strategy. Keeping track of all the multidisciplinary aspects of this exercise is a real challenge. One of the most important questions to be answered at this stage is how the final targeted EMC performance can be translated into a targeted EMC specification at e.g. block-level or package-level.

During the validation phase, one is often confronted with evolved or new requirements, new insights and issues which were not observed in simulation or taken into account in the initial risk assessment. This implies a need for sufficient flexibility in the design and test strategies. Adapting the design and test plans should however be well controlled, and the question how one will respond to such changes in a product's life cycle should already have been answered at the definition phase of the product.

Finally, an IC product will be applied in a larger module or system. A sensor might be immediately connected to a wire harness, or might end up in a module or on a PCB. Although the module supplier should conduct his own EMC aware design flow, it is the IC supplier who needs to share guidelines for the IC's integration in the application. This means that the applied simulation and test strategy should be in line with the final application of the product.

A solid requirement definition rolls out as a red carpet through the different product development phases. The full set of practices, methods and tools guide the development process in order to have the final product behaving as expected within the ambient electromagnetic environment. Subsequently, the time to market, the development cost, and the number of customer returns can be minimized.

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## 10<sup>th</sup> March 2022 TECHNICAL SESSION : IC Emission 2

Chair : **Dr. ing. Tim Claeys, KU Leuven, Belgium**

**Mr. Alexandre Boyer, LAAS-CNRS, France**

### 11h15

#### Accurate test method and comparison based on TEM cell and IC- Stripline TEM cell

Chen Ledong<sup>1</sup>, Wu Jianfei<sup>1,2</sup>, Zhang Hongli<sup>2</sup>, Gui Xinhai<sup>3</sup>, Zheng Yifei<sup>1</sup>, Zhang Heng<sup>3</sup>

<sup>1</sup>National University of Defense Technology, China, People's Republic of ; <sup>2</sup>Tianjin Binhai Civil-military Integrated Innovative;

<sup>3</sup>Unit 93088 of PLA

#### Abstract:

Integrated Circuit (IC) radiation emission problems are becoming demanding challenges under the traction of Moore's Law due to configuration complexity and vast computational resources. This paper improves the test methods of TEM cell and IC-Stripline TEM cell and compares the difference between the two on the chip radiation emission measurement. Test boards complying with the IEC61967-2 and IEC61967-8 standards were designed to complete the test. And the test results after the improved test method are more accurate than the test results of the traditional method. The test results of the TEM cell and the IC-Stripline TEM cell reflect the differences between the two devices and provide a reference for selecting test devices before chip testing.

### 11h35

#### EM Emission modeling for secure IC design

Davide Poggi<sup>1,2</sup>, Philippe Maurine<sup>2</sup>, Thomas Ordas<sup>1</sup>, Alexandre Sarafianos<sup>1</sup>, Jeremy Raoult<sup>3</sup>

<sup>1</sup>STMicroelectronics, France ; <sup>2</sup>LIRMM, France ; <sup>3</sup>IES, France

#### Abstract:

For some decades now, electromagnetic radiations have not only generated electromagnetic compatibility problems but are a critical threat also for secure IC designers. In fact, these radiations can be collected, with an EM probe, to perform electromagnetic side-channel attacks (EM SCA), in order to retrieve secure data from ICs. Within this context, this paper aims to propose an industrial simulation flow able to reproduce the EM emissions of ICs during the design stage. It also proposes a technique allowing to correctly identify EM leakages prior to fabrication, considering the absence of noise in simulated traces. Finally, attacks performed with horizontal and vertical probes are compared, as well as front-side and back-side analyses, in order to demonstrate that only upper metal layers need to be considered to model the magnetic field captured by an EM probe placed close to the IC surface.

### 11h55

#### Near field Measurements of Sub-millimeter-wave Noise Emission from Digital Integrated Circuits

Koh Watanabe, Takuya Wadatsumi, Kazuki Monta, Mai Aoi, Misaki Komatsu, Ryota Sakai, Satoshi Tanaka, Takuji Miki, Makoto Nagata

Kobe University, Japan

#### Abstract:

The 5th generation (5G) communication system exploits millimeter-wave (mm-wave) frequency bands for highspeed and large-capacity cellular communication. The sub-mm wave communications have to conquer substantial challenges to hold a necessary receiver (Rx) and transmitter (Tx) sensitivity because of large path losses and cable losses, compared to sub-6 GHz ones. In addition, baseband digital integrated circuits (ICs) operate at the clock frequency of GHz and emanate electromagnetic (EM) noises in a very wide range of frequency, which can degrade the 5G performance in the sub-mm-wave band. This paper exhibits the presence of high-order harmonics of such digital switching noises in sub-mm-wave bands, from 22 GHz to 30 GHz. The near-field EM noise measurements that use a sub-mm-wave down converter are demonstrated. It is shown that the emission noise from digital ICs can be the root cause of EM interference in a cellular system using 30 GHz or larger.

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## 10<sup>th</sup> March 2022 TECHNICAL SESSION : DESIGN TECHNIQUES 2

Chair : **Prof. em. dr. Johan Catrysse, KU Leuven, Belgium**

**Mr. Adrijan Baric, University of Zagreb, Croatia**

**13h30**

### **Meta-Stability of Behavioural Models of Integrated Circuits with DC and RF Sub-Models**

Marko Magerl<sup>1</sup>, Christian Stockreiter<sup>1</sup>, Adrijan Baric<sup>2</sup>

<sup>1</sup>ams OSRAM Group, Austria ; <sup>2</sup>University of Zagreb Faculty of Electrical Engineering and Computation, Croatia

#### **Abstract:**

A black-box model architecture with separate DC and RF sub-models is presented that enables building accurate behavioural models of nonlinear integrated circuit blocks for time-domain (transient) simulations with or without an initial condition file. The methodology for separating the DC and RF behaviour of the modelled circuit is presented in Verilog A. The nonlinear RF sub-models are built using echo state networks (ESN). The meta-stability of the model operating point in the large-signal simulation is observed as a function of the ESN characteristics, and a test for model meta-stability is defined. The behavioural model accuracy in the top-level simulation is quantified and the presented methodology is evaluated on a voltage reference test case.

**13h50**

### **Determination of Equivalent Coupling Surface of Ferrite Beads and related Filter Design Stakes for Multi-Sourcing**

Marine Stojanovic, Frédéric Lafon, Priscila Fernandez-Lopez, Kevin Loudiere, Catalina Vasquez-Hormazabal

Valeo, France

#### **Abstract:**

The risk of shortage and multi-sourcing for all electronic components has increased in the last few years and will speed up in the coming years. In order to limit this risk, a strategy for reducing the EMC requalification of products, when components reference are changing, has been developed. The equivalence of products, in terms of EMC performances, is now shifted from product level to component level in order to avoid redoing a complete qualification on product. It means that, if components are equivalent in terms of EMC performances, products will be considered as equivalent. For the definition of an equivalence between two components, one of the key parameters is the equivalent coupling surface, that corresponds to its capability of coupling a magnetic field. The methodology for equivalent coupling surface determination of ferrite beads is, thus, presented in this paper. That procedure is based on TEM (Transverse ElectroMagnetic) cell measurements. All the related stakes regarding the particular structure of ferrite beads and regarding filter design are also presented in this paper.

**14h10**

### **Equivalent circuit of Common-Mode Choke Coil Considering with conversion from Differential-Mode signal to Common-Mode Disturbance**

Nobuo Kuwabara, Tohlu Matsushima, Yuki Fukumoto

Kyushu Institute of Technology, Japan

#### **Abstract:**

A common-mode choke coil (CMC) is an essential device for achieving electromagnetic compatibility (EMC). An equivalent circuit considering the common-mode (CM) disturbance converted from differential-mode (DM) signal is needed because the spectrum of telecommunication signals overlaps with the regulated frequency band of the radiated disturbance due to the increase of telecommunication speed in recent years. In this paper, an equivalent circuit of CMC considering the conversion phenomenon is proposed. The admittances were inserted between each terminal of the CMC and the ground for demonstrating the phenomenon. The SPICE model of CMC was represented by the combination of the ABCD chain-parameter-matrices, and the elements of the overall matrix were calculated. The mixed-mode S-parameters were calculated using these elements. The elements of the ABCD matrix and the mixed-mode S-parameters were measured and the admittance values were determined by comparing the calculated data with the measured data. The pulse response calculated by the proposed equivalent circuit was well agreed with the measurement value.



**14h30**

### Implementation of an EMC modeling and simulation methodology applied on a embedded LINphy module

Younes Benlakhouy

*NXP Semiconductors, Germany*

**Abstract:**

In order to consider the EMC behavior of a module during design phase, simulations have to be done. This study concentrates on two standard EMC tests (Conducted Emission and Direct Power Injection) for doing measurements and simulations on a LINphy module. The results are compared and the simulations are adapted for a good correlation to the measurements and a short simulation time. Finally, a simulation methodology is concluded.

## 10<sup>th</sup> March 2022 TECHNICAL SESSION : IC Immunity 1

Chair : **Dr. ing. Dries Vanoost, KU Leuven, Belgium**

**Mr. Franco Fiori, Politecnico di Torino, Italy**

**15h20**

### EMC related Handle-Wafer Backside Effects in a 180nm SOI-Technology

Dirk Michael Nuernbergk<sup>1</sup>, Mario Knoll<sup>1</sup>, Klaus Heinrich<sup>2</sup>, Burak Baran<sup>1</sup>

<sup>1</sup>Melexis GmbH, Germany; <sup>2</sup>X-FAB Global Services, GmbH

**Abstract:**

During EMC measurements of a CAN (Controller Area Network) transceiver integrated circuit (IC) it was found that the bandgap circuit showed a significant voltage drop for low frequencies in a range of 1 MHz to 20 MHz. Standard methods to investigate or simulate direct power injection on the supply pins of the bandgap circuit failed and did not show the expected dip of the bandgap voltage mean value. A detailed investigation was started to find the root cause of the effect. It turned out that the bandgap was influenced by capacitive coupling from the handle wafer underneath the buried oxide of the IC. The methodology to find such a handle wafer effect of 180nm SOI technology is described in this paper.

**15h40**

### Investigation on the Susceptibility to EMI of Second-Order $\Delta\Sigma$ Modulators

Markljan Fishta, Franco Fiori

*Politecnico di Torino, Italy*

**Abstract:**

This paper analyzes the effects of radio frequency interference on second order  $\Delta\Sigma$  modulators based on continuous-time (CT) and on discrete-time (DT) architectures. Specifically, Modulators used for the acquisition of sensor signals are targeted, which can operate with moderate clock rates due to the relatively small bandwidth of the signal to be acquired. A continuous wave interference with frequency above that of the modulator clock signal is superimposed onto the nominal input one with the purpose of evaluating the degradation of their performance, and more specifically their capability to demodulate out of band interference.

**16h00**

### A Technique to Assess Conducted Immunity of an Electronic Equipment after an Obsolete Integrated Circuit Change

Saliha Chetouani<sup>1,2</sup>, Alexander Boyer<sup>2,3</sup>, Sonia Ben Dhia<sup>2,3</sup>, Sebastein Serpaud<sup>1,2</sup>, Andre Durier<sup>2,4</sup>

<sup>1</sup>IRT Saint Exupéry, France ; <sup>2</sup>LAAS-CNRS, France ; <sup>3</sup>Uni.de.Toulouse, INSA, France ; <sup>4</sup>Continental Automotive, France

**Abstract:**

This paper describes a fast methodology for managing the obsolescence issues of integrated circuits in industrial equipment (aeronautical or automotive). The objective is to predict EMC non-compliance risk, especially for conducted immunity, after a component change. Based on black box modeling using S-parameters, this experimental approach consists in declining the conducted immunity requirements, from the input of the equipment to the pins of the replaced component. Once this transfer function is established, a link is envisaged between the immunity level determined at the boundary of the component to be replaced and that of the new one. This link allows the prediction of EMC non-compliance risk level, from an equivalent test at the component level, due to a change of a component.



**16h20**

### **Communication Noise Investigation on Automotive Sensor**

Adrien Doridant, Kamel Abouda, Jalal Ouaddah, Marianne Maleyran, Phillippe Calmettes, Jerome Enjalbert, Jinbang Tang  
*NXP Semiconductors*

**Abstract:**

During the electrical characterization of a sensor integrated circuit, communication noise was observed on the accelerometer data. In automotive environment, where personal safety must be ensured at all times and under all circumstances, signal integrity must be guaranteed with a very high level. In this paper, first the cause of this interference is studied. Secondly, electrical and electromagnetic simulations coupled with experiments were set up in order to understand and predict communication noise issue.

## **10<sup>th</sup> March 2022 DISCUSSION FORUM**

**Chair : Prof. dr. ir. Davy Pissoort, *KU Leuven, Belgium***  
**Dr. Ramiro Serra, *TU Eindhoven, Netherlands***

**16h40**

### **EMC Design Chaos**

Mart Coenen

*EMCMCC, Netherlands*

**Abstract:**

Ever since the introduction of the EMC requirements in 1992 (for Europe), electronic designs have taken a massive growth in a broad variety of industry. Now, 30 years later, over a 1000 internationally agreed EMC related standards apply for the various products, from ICs, package design, PCB to large systems and installations. Most of the IC developments result from stepwise changes in the design, like further integration; from  $\mu\text{m}$  to nm-scale, circuit improvements, larger densities, faster processes, application extension, etc. At the product level, the EMC requirements have hardly changed, except for the extension of the frequency ranges up into the GHz ranges. Every excess of an RF emission limit means a 'non-conformity' and should result in a non-release of the product to the market. The excess of an RF emission limit often results from severe resonances occurring with nearly every level of circuit design, decoupling population of PCBs, filtering, cabling and enclosures. The likelihood for passing the EMC requirements at once remains a challenge with poor reproducibility as a result. In this paper, the various levels at which these resonances may occur will be described, together with their possible solutions.

**17h05**

### **The Billion Dollar Mistake**

Daniel Lee Beaker

*NXP Semiconductors, USA*

**Abstract:**

Engineering teams around the world are facing increasingly difficult challenges to design electronic products and achieve good signal integrity and compliance. However, the status quo had become to expect the design to fail EMC testing, and not just once, but three, four, or as many as five times. Each time the design is sent to be retested, there is little confidence in success. This cycle is expensive in both the time it takes to redesign the product and the cost of expediting fabricating the new PCB and assembly. Add this to the cost of retesting the product, and the numbers add up very quickly. This expense and delay in product certification are not in the budget or the schedule. The expense directly affects the bottom line of the electronic supply company but also affects the customers waiting for the product. Instead of designing the next big thing, teams are trying to fix the current one. Billions of dollars are lost each year designing products that are expected to fail.



## 11<sup>th</sup> March 2022 TECHNICAL SESSION : IC Immunity 2

Chair : **Dr. ing. Dries Vanoost, KU Leuven, Belgium**

**Mr. Jan Niehof, NXP**

**9h30**

### **EMC Sensitivity Analysis of Crystal Oscillator through Direct Power Injection (DPI)**

Sachin Bansal, Anand Sinha, Avinash Tripathi, Sanjay Wadhwa, Rishi Bhooshan, Robert Lippmann, Younes Benlakhrouy  
*NXP Semiconductors*

**Abstract:**

Crystal oscillators, owing to their high-stability output, usually act as the primary clock of a system PLL. To ensure that the system clock remains robust, the oscillator-generated clock should maintain a stable frequency. This makes it crucial to ensure that connections to the off-chip crystal unit are immune to EMC noise. This work presents a simulation methodology for Direct Power Injection for checking EMC robustness of crystal oscillators. The analysis has been done on NXP's automotive microcontroller devices and results have been presented.

**9h50**

### **IEMI Fault Injection Method using Continuous sinusoidal Wave with Controlled Frequency, Amplitude, and Phase**

Hikaru Nishiyama<sup>1</sup>, Daisuke Fujimoto<sup>1</sup>, Youngwoo Kim<sup>1</sup>, Hideaki Sone<sup>2</sup>, Yu-ichi Hayashi<sup>1</sup>

<sup>1</sup>Nara University of Science and Technology, Japan ; <sup>2</sup>Tohoku University, Japan

**Abstract:**

A fault injection attack based on an intentional electromagnetic interference (IEMI) using a continuous sinusoidal wave can generate a fault that is applicable for the differential fault analysis (DFA) against cryptographic module non-invasively. However, previous studies often generate multi-byte faults in the output ciphertext which are not applicable for the DFA, and they increase the analysis time dramatically. In this paper, we propose an IEMI-based fault injection method that can increase the occurrence of a one-byte fault in the output ciphertext by controlling the frequency, phase, and amplitude of the injected sinusoidal wave. Specifically, we control the frequency and phase of the sinusoidal wave injected into the cryptographic module implemented with the advanced encryption standard (AES). At the same time, the number of faults of the output ciphertext is monitored so that a glitch is generated in phase at each rising edge of the clock. At this condition, the amplitude is controlled to further increase the timing difference between the rising timing of the original clock and the overclocking occurrence timing associated with the glitch. Experimental results validated that the proposed method can increase the ratio of the number of one-byte faults to the number of faults. From the experimental results, we discuss a direction to further improve the method to maximize 1-byte faults for the future study.

**10h10**

### **New Method for testing the susceptibility to intermodulation of RF systems**

Alain Grezes<sup>1,2</sup>, Jeremy Raoult<sup>2</sup>, Alexandre Martorell<sup>1</sup>

<sup>1</sup>Thales SIX GTS, France ; <sup>2</sup>IES - University of Montpellier, France

**Abstract:**

The susceptibility of RF devices to the third order intermodulation (IM3) is studied. In this paper, we propose an alternative of the classical two-tone test by using tones of not equal amplitude injected on RF devices. This new method aims at enhancing the intermodulation distortion characterization. We evaluate this method by measuring in a conducted mode the IM3 responses reflected by RF systems, namely a modem and a walkie-talkie.

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## 11<sup>th</sup> March 2022 TECHNICAL SESSION : **PETER Project**

**Chair : Mr. Qazi Mashal Khan, ESEO, France**

**Dr. Mohsen Koohestani, ESEO, France**

**10h40**

### **Comparing Simulated Impact of Single Frequency and Multitone EMI for an Integrated Circuit**

Lokesh Devaraj<sup>1</sup>, Qazi Mashal Khan<sup>2</sup>, Alastair Ruddle<sup>1</sup>, Alistair Duffy<sup>3</sup>

<sup>1</sup>Horiba Mira Limited, UK ; <sup>2</sup>ESEO/INSA Rennes, France ; <sup>3</sup>De Montfort University, UK

**Abstract:**

Electromagnetic immunity performance characteristics for integrated circuits are currently verified using tests involving single-frequency continuous wave disturbances. In real operational environments, however, systems may be exposed to simultaneous interference sources at multiple frequencies. Simulation results obtained for the electromagnetic susceptibility of a simple voltage-controlled oscillator to randomly generated multitone interference are compared with corresponding data obtained for single frequencies. The results obtained are used to assess the validity of the current approach of testing circuit designs for immunity using single frequency noise source. Notable differences in the output response of the circuit to single and multitone interference, which could possibly lead to system malfunctions, are illustrated.

**11h00**

### **A new TRL/TRM PCB-based Calibration Method for On-Board Devices Under Test (DUTs)**

Akram Ramezani<sup>1</sup>, Qazi Mashaal Khan<sup>2,3</sup>, Hugo Pues<sup>1</sup>

<sup>1</sup>Melexis, Belgium ; <sup>2</sup>ESEO, France ; <sup>3</sup>INSA Rennes, France

**Abstract:**

In this paper, a new TRL/TRM calibration method is described and compared to an electronic calibration module (ECal) method which is widely used in industry. This method needs a specifically made de-embedding board but does not require an expensive ECal or any special precision board-level calibration devices. The method is applied to an automotive sensor interface IC showing the new calibration method enables us to conduct accurate on-board S-parameter measurements up to 4 GHz whereas the other method becomes inaccurate above 500 MHz.

**11h20**

### **Digital and Analogue Hardware Design of an On-Board EMI detector**

Hasan Habib<sup>1</sup>, Tim Claeys<sup>1</sup>, Richard Perdriau<sup>2</sup>, Davy Pissoort<sup>1</sup>

<sup>1</sup>KU Leuven, Belgium; <sup>2</sup> ESEO, France

**Abstract:**

The conceptual design of an EMI detector based on a pair of transmission lines sending inverted data has been presented previously. This paper focuses on the actual hardware design of such an EMI detector. The prototype of the EMI detector is implemented using both analogue and digital hardware designs. In the analogue design, the EMI detector detects the presence by processing the signal at the receiver end directly using analogue electronic components. In the digital design, the EMI detector uses an analogue to digital converter (ADC) to convert the voltage signal from the receiver end into its digital form. This voltage is further processed using a Field Programmable Gate Array (FPGA), which generates a warning when EMI is present. This paper compares the operation and performance of both designs of the EMI detector in a harsh electromagnetic (EM) environment.

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**11h40**

### **A Comparison among DPI Immunities of Multi-Stage CSVCOs and Ring Oscillators**

Qazi Mashaal Khan<sup>1,2</sup>, Akram Ramezani<sup>4</sup>, Mohsen Koohestani<sup>1,3</sup>, Mohamed Ramdani<sup>1,3</sup>, Richard Perdiau<sup>1,3</sup>

<sup>1</sup> ESEO, France ; <sup>2</sup> INSA Rennes, France ; <sup>3</sup> IETR, France ; <sup>4</sup> Melexis, Belgium

**Abstract:**

This paper evaluates & compares, through electrical simulation, the immunity of multi-stage current starved voltage controlled oscillators (CSVCOs) and ring oscillators (ROs) submitted to direct power injection (DPI). All circuits were designed and simulated in the 180 nm 5 V XFAB-SOI process, with matching dimensions. The failure criteria selected were the output frequency, peak-to-peak voltage and DC offset voltage. Results demonstrated, that CSVCOs were susceptible at lower DPI frequencies, while the ROs were susceptible at higher frequencies. Both were impacted by different failure criterions. Regardless of the oscillator category, a higher number of inverter stages resulted in lower susceptibility to incident power levels. As a consequence of increasing the power level of RF injections, the highest DC supply current and output power, monitored for each oscillator was close to their nominal output frequencies. These circuits are currently being fabricated in a test chip and immunity measurements will be performed on it.

## **11<sup>th</sup> March 2022 TECHNICAL SESSION : New Design Methodologies**

**Chair : Dr. ing. Tim Claeys, KU Leuven, Belgium**

**Dr. Anne Roc'h, TU Eindhoven, Netherlands**

**13h00**

### **Analysis of Filtering Window Impacts on Estimation Accuracy of Information Leakage from Exposed Power Delivery Network of Cryptographic Devices**

Youngwoo Kim, Shinpei Wada, Daisuke Fujimoto, Yuichi Hayashi

*Nara Institute of Science and Technology, Japan*

**Abstract:**

In this paper, an analysis of filtering window impacts on estimation accuracy of electromagnetic (EM) information leakage from exposed power delivery network (PDN) of cryptographic devices is presented. There are exposed areas in the PDN such as decoupling capacitors, through via plating, and small power/ground interconnections where full-byte secret key information can be leaked via EM field radiation. Various waveforms are measured using EM field probes on the PDN of the target cryptographic device. Correlation electromagnetic analysis (CEMA), field distribution analysis, and secret key extraction are conducted based on the measured waveforms via EM field radiation from the exposed PDN. It is verified that adopting a proper filtering window to remove impacts of noise irrelevant to secret key processing is important for an accurate and efficient estimation of the information leakage from the PDN. Based on the measurement and analysis results, an efficient EM information leakage estimation method based on the dominant field radiation obtained from filtered waveforms is discussed.

**13h20**

### **A Fault Tree Approach Focusing on Electromagnetic Interference**

Klaus Hörmaier<sup>1</sup>, Hubert Zangl<sup>2</sup>, Daniel Kircher<sup>3</sup>, Bernd Deutschmann<sup>3</sup>

<sup>1</sup> Infineon Technologies, Austria ; <sup>2</sup> Alpen-Adria Universität Klagenfurt, Austria ; <sup>3</sup> Graz University of Technology, Austria

**Abstract:**

Compatibility with respect to Electromagnetic Interference (EMI) is an important property of all electric and electronic systems. Consequently, functional safety standards require that EMI is considered. In contrast to other properties, EMI is usually not treated in a statistical sense, i.e. a system is considered compatible if it succeeds to withstand a certain level of disturbances. This paper aims to discuss this approach and suggests to differentiate two types of interferences. The first type, which is the normal EMI and which is typically of comparatively low power, may occur at any time during normal operation. Consequently, the system has to fully comply with such disturbers. The second type of EMI is caused by component failures. This type of disturbances is responsible for high power levels. However, as it is only present in case of component failures, it may be treated similar to other faults in the system. We describe how this approach allows for integrating interference caused by component faults into a Fault Tree Analysis of the system.



**13h40**

### **EMC Methodology to Optimize Application of Electronic Component Multisourcing**

Kevin Loudiere, Frédéric Lafon, Priscila Fernandez-Lopez, Jean-François Léon, Marine Stojanovic

*Valeo, France*

**Abstract:**

This paper introduces a way to reduce product EMC requalification when new sources are introduced. The strategy is to shift the qualification from the product to the component itself considering that if the component are equivalent, the products behavior will also be the same. For each component category (capacitor, inductor, diodes, IC...), we first identify the relevant characteristics to be considered for the comparison and impacting the EMC performance of a product ( $Z(f)$ ,  $I(V)$ ...). Criteria are then defined, based on technology, geometric parameters, tolerances and measurement uncertainties. An application on X7R capacitor is given to illustrate this methodology. Limits of the method and application on complex component will then be introduced (In final version of the paper).

**14h20**

### **Analysis of the Impact of Artificial Networks in System-level EMC tests**

Pablo J. Gardella<sup>1,2</sup>, Eduardo Mariani<sup>1,3</sup>

<sup>1</sup> Allegro Microsystems, Argentina; <sup>2</sup> Instituto Tecnológico de Buenos Aires; <sup>3</sup> EM Ingenieria, South America

**Abstract:**

The impedance of an Off-The-Shelf Artificial Network (OTS-AN) and a custom made High-Frequency Artificial Network (HF-AN) were analysed and compared. It is showed that in order to meet the requirements of automotive standards, such as Bulk Current Injection (BCI) from ISO 11452-4 as well as both Conducted and Radiated Emissions (CE, RE) from CISPR 25, the HF-AN is needed. System-level circuit simulations were run using S-parameters for quantifying the impact of these two models in the previously mentioned EMC tests. Above 50 MHz, up to 3.5 dB and 4.3 dB differences were found on the transfer-impedance of CE and in the Common-Mode to Differential-Mode conversion of BCI, respectively. On the other hand, in RE the OTS-AN led to an overestimation of the emission profile in the 300 MHz and 800 MHz band as high as 5.3 dB. Besides that, it is showed that the OTS-AN behaves as a source of non-constant uncertainty, specially above 50 MHz. Finally, the issues in terms of reproducibility, repeatability and accuracy that arise from the non-RF connectors in the OTS-AN are discussed and a metric for test-bench comparison and validation is proposed.

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**11<sup>th</sup> March 2022 15h - TUTORIAL SESSION**

**“Board-Level-Shielding (BLS)”**

**Prof. Dr. Andy Marvin, University of York, UK**

**Chair: Prof.dr.ir.Davy Pissort, KU Leuven, Belgium**

**Prof. em. dr. Johan Catrysse, KU Leuven, Belgium**



Andy Marvin is Professor Emeritus at the University of York and a Leverhulme Foundation Emeritus Fellow. He was the founding Technical Director of York EMC Services Ltd, now Eurofins York, and was until December 2017 the Professor of Applied Electromagnetics, in the University of York's Department of Electrical and Electronic Engineering. He was Vice-Chairman of the IEEE Std-299 Working Group on Shielding Effectiveness Measurement, and was also Vice-Chairman of the IEEE EMC Society Standards Advisory and Co-ordination Committee. From 1994 to 2015 he was an Associate Editor of IEEE Transactions on EMC. He has contributed lectures on Antennas and on Shielding to the IEEE EMCS Global University and Chaired its Faculty in 2010. He is a founder member of the International Steering Committee of EMC Europe conferences, Conference Co-Chair of EMC Europe 2011 (York) and Chair of the International Steering Committee from 2015 – 2018. His main research interests are EMC measurement and modelling techniques, EMC antennas and electromagnetic shielding measurement and modelling. To date, starting in 1976, he is an author on over 300 papers.

**Abstract:**

Shielded enclosures installed on circuit boards are fundamentally different to larger shielded enclosures. Typically they have only five sides, the sixth side being the circuit board ground plane to which the shield is soldered. They are also much smaller than conventional shielded enclosures with dimensions in the tens of mm range. Board level shields are typically installed within a larger shielded equipment enclosure or in close proximity to antennas. These constraints make the measurement of the shielding effectiveness of board level shields challenging. As part of the IEEE P2716 project we have been working on techniques to measure how effective these shields are. The talk will concentrate on our new measurement techniques which include statistical descriptions of the shielding rather than simple shielding effectiveness figures in order to address the added complexity of the board level shields' external environment. The latest work on measurements using attachment techniques other than soldering will also be described.



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## VOTE OF THANKS

Chair: **Prof.dr.ir.Davy Pissoort, KU Leuven, Belgium**

### Dear participant of EMC COMPO 2021

A warm “thank you” to all who participate at this virtual EMC COMPO 2021. We hope that you had an interesting symposium and found insights regarding your own research and development work in progress.

Thanks to the keynote speakers, the speakers of the plenary sessions and the panel members of the discussion forum, who shared their vision on the future challenges regarding the development of new generations of ICs and the related EMC issues.

Thanks to the local organizing committee, who did a huge work in transforming the symposium from a physical into a virtual one. We would especially like to mention Stephane Stroobant and Dr. Tim Claeys. Without their dedication, this virtual edition would have never been possible. Thanks to the program committee and all exhibitors who supported this symposium.

Thanks to you all, who presented a paper in one the technical sessions and sharing your latest research results during this symposium, and to all over the world, who participated at EMC COMPO 2021.

We hope to welcome you from person-to-person at the next EMC COMPO 2023!

And ... do not forget to visit our historical medieval city of Bruges, virtually at [Virtual Brugge, the official Poppr 360 virtual tour of Bruges \(virtualbruges.com\)](#) or physically in the future?

Prof. Davy Pissoort (Chair of EMC COMPO 2021)

Prof. em. Johan Catrysse (Vice-chair of EMC COMPO 2021)